Thermocouple interfaces to serial port

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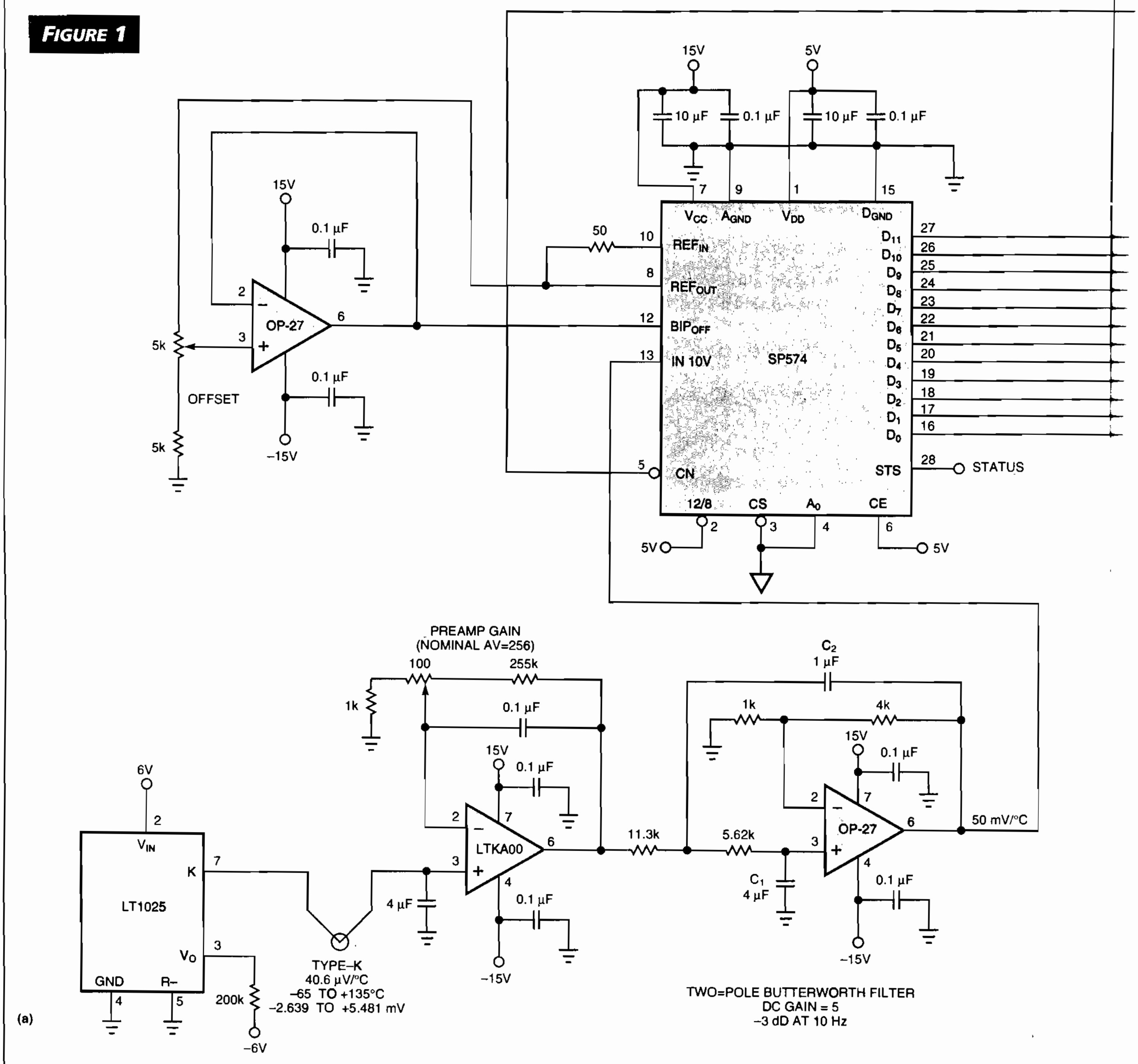
The circuit in **Figure 1** acquires temperature data via an IBM PC serial port using a thermocouple-based sensor. The sensor is a type-K (chromel-alumel) thermocouple. When in contact, the dissimilar metals produce a potential difference that is a function of temperature. Additional thermocouple junctions form where the chromel and alumel make contact with the copper connections of the signal-conditioning circuitry. Thermocouple measurements

FIGURE 1

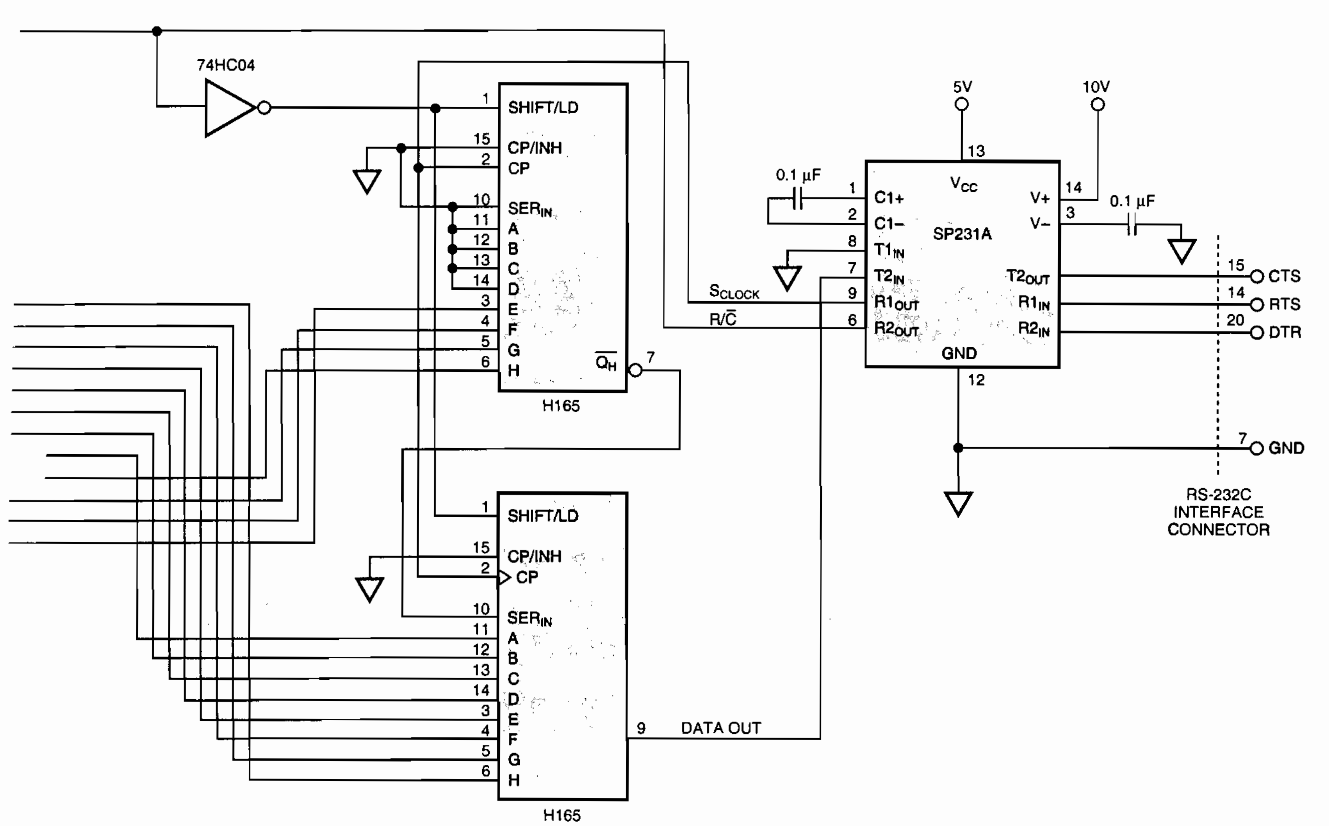


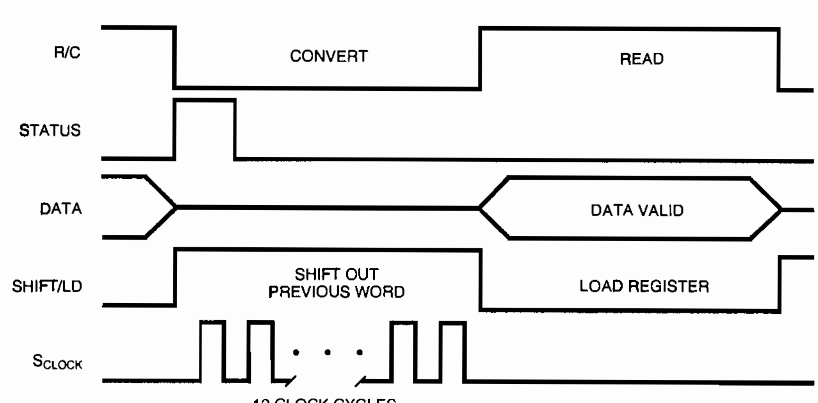
NOTE: C1 AND C2 MUST BE POLYSTYRENE, MYLAR, OR MICA.

re inherently differential. Placing the incidental (chromel-nd alumel-copper) thermocouple junctions in an ice bath raditionally maintains the reference junction.

In this circuit, the LT1025 cold-junction compensator provides the signal conditioning. The compensator's voltage varies with the temperature of the reference junction in such a way that when summed with the thermocouple voltage, the combination behaves as if the reference junction were maintained at 0°C. (You should place the compensator as close as possible to the reference junction.) The compensator also linearizes the output of the thermocouple and is markedly more convenient than an ice bath.

The LTKA00 thermocouple amplifier provides gain adjustment. A two-pole Butterworth filter provides noise reduction





(b)

Using a cold-junction compensator, a thermocouple amplifier, a filter, an ADC, and parallel-to-serial shift registers, this circuit (a) interfaces a type-K thermocouple with an RS-232C port. The port's DTR signal controls the ADC's R/C line to initiate a conversion (b).

and scales the applied signal to the ±5V input range of the SP574 ADC. The circuit adjusts for offset by applying a buffered fraction of the converter's internal reference voltage to the bipolar offset pin.

A falling edge on the read-convert bar (R/C) of the ADC initiates a conversion (**Figure 1b**). With R/C low, the shift-load pins (SHFT/LD) of the 74HC165 parallel-in/serial-out shift registers are high. This high level places the registers in shift mode, so that the circuit can shift out the previous conversion's data. When R/C goes high, the registers load an updated conversion.

The SP231A RS-232C driver/receiver contains a charge pump and produces the required RS-232C output levels from a 5V supply. The data-terminal-ready (DTR) signal toggles R/C. The request-to-send (RTS) signal produces the clock signal used by the shift register (S_{CLOCK}). The data output from this register toggles the clear-to-send (CTS) signal.

The accompanying Quickbasic program, which you can download from **EDN BBS /DI_SIG #1782,** writes and reads these digital signals and produces appropriate delays to allow the ADC sufficient time for a conversion. (DI #1782)

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Carry-save addition saves logic and time

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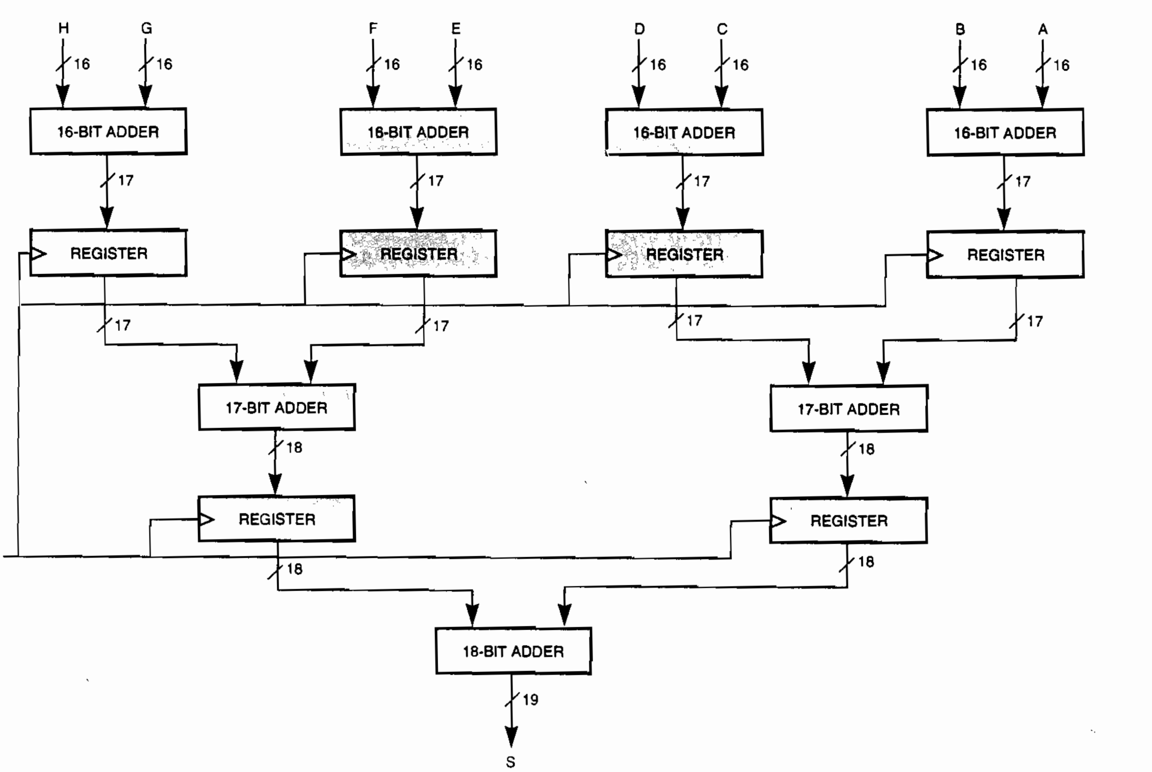
Summing multiple operands is a common operation in signal-processing applications. One such application requires summing eight 16-bit operands to generate a 19-bit result. To achieve the required setup time (t_S) and clock-to-output time (t_{CO}) in the system, you need pipelining. **Figure 1** shows the straightforward way to implement this multiple-

FIGURE 1



A straightforward multiple-operand addition requires two levels of pipelining registers to achieve the needed setup and clock-to-output times for the system.